PARALLEL MACHINES

ARCHITECTURE

CLASSIFICATION COULD BE ACCORDING TO

MEMORY MODEL

HOW CPU VIEWS AVAIALBE MEMORY ?

SHARED MEMORY

DISTRIBUTED MEMORY

SHARED MEMORY MODEL

SHARED MEMORY MODEL

SINGLE

ADDRESS SPACE

ALL PROCESSORS HAVE ACCESS TO POOL OF

SHARED MEMORY

ALSO CALLED

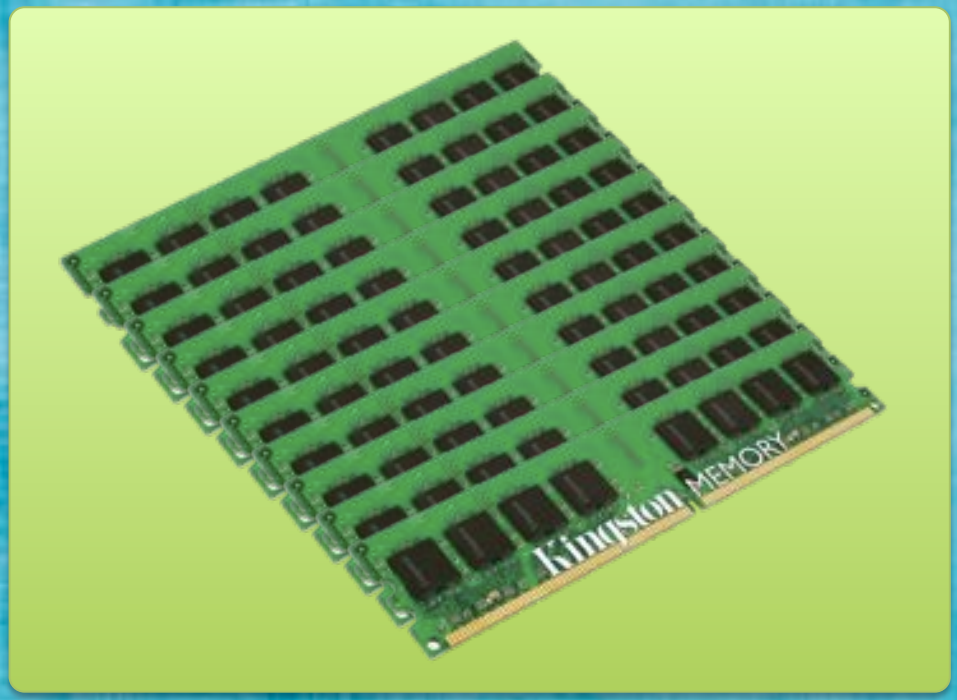
MULTI-PROCESSORS

HPC SYSTEM (MPs)

SHARED MEMORY MODEL

MULTI PROCESSORS

GLOBAL MEMORY SPACE



DISTRIBUTED MEMORY MODEL

MULTIPLE ADDRESS SPACES

EACH PROCESSORS HAVE ACCESS TO ITS OWN

LOCAL MEMORY

MUST DO MESSAGE PASSING TO EXCHANGE DATA BETWEEN PROCESSORS

DISTRIBUTED MEMORY MODEL

DISTRIBUTED MEMORY MODEL

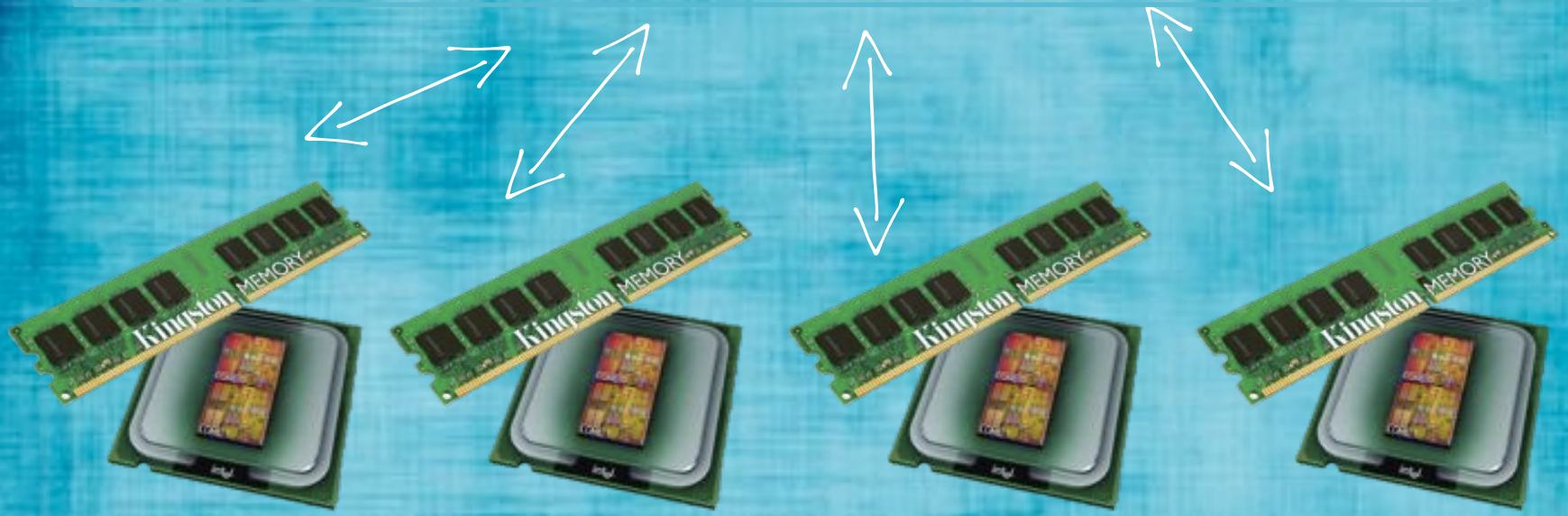
MULTI COMPUTERS

CLUSTERS

DISTRIBUTED COMPUTING

INDEPENDENT MACHINES
LOOSELY COUPLED BY A
SCHEDULER
TO SOLVE A
COMPLEX COMPUTATIONAL
PROBLEM

Inter-Processor Connection Mechanism



MODERN CLUSTERS ARE EVEN MORE COMPLEX (HYPRID)

GRID COMPUTING

INDEPENDENT MACHINES
LOOSELY COUPLED
COMBINED INTO A
UNIFIED SYSTEM BY
SOFTWARE
NETWORKING

TERMINOLOGY SO FAR

SHARED MEMORY

DISTRIBUTED MEMORY

COMMUNICATIONS

SYNCHRONIZATION

PARALLEL OVERHEAD

SCALABILITY

CLUSTER COMPUTING

HETEROGENEOUS COMPUTING

DEFINITION

SYSTEM
COMPOSED OF DIFFERENT
HETEROGENOUS
COMPUTATIONAL UNITS

IN GENERALL

COMPUTATIONAL UNITS PROCESSORS
DIFFERENT ISAs
INSTRACTION SET ARCHITECTRES

A HETEROGENOUS SYSTEM COULD BE COMPOSED OF MIX OF CUs

1 GENERAL PURPOSE PROCESSOR (GPP)

2 SPECIAL PURPOSE PROCESSOR (SPP)
* DIGITAL SIGNAL PROCESSOR (DSP)
* GRAPHICS PROCESSING UNIT (GPU)

3 CO – ROCESSOR

4 CUSTOM ACCELERATION LOGIC
* ASICs
* FPGAs

Wrap Up

Incoming presentations
will be more detailed

Thanks For Paying Attention